UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/570,839	12/18/2006	Theodor Doll	3222.1430000	8784

26111 7590 02/23/2010

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
SUCH, MATTHEW W	

ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
02/23/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/570,839	DOLL ET AL.	
	Examiner	Art Unit	
	MATTHEW W. SUCH	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,13 and 19-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,13 and 26* is/are allowed.

6)☒ Claim(s) *19-25,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 19-25 and 27-28 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Independent claims 19 and 23 each recite "wherein the first and second thicknesses are at least approximately twice the third thickness". This is not supported by the disclosure originally filed. The closest teachings in the specification and drawings indicate that "a second vapor-metal layer 504 is deposited to the entire surface" and shown as two layers in Figure 5. However, the specification and the drawings are totally devoid of any teachings of the relative thicknesses of the first and second electrodes relative to the third electrode by either direct disclosure or inherency. A mere teaching of "a second vapor-metal layer 504 is deposited to the entire surface" does not support a claimed limitation of "wherein the first and second thicknesses are at least approximately twice the third thickness" since there is no teaching of how thick the second vapor-metal layer is relative to the first vapor-metal layer.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19-22 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (`935) in view of Mizusaki (WO `640; supplied with Office Action dated 11 September 2009) in view of Hirai (`900).

a. Regarding claim 19, Zhang teaches an electronic component as a bottom gate transistor with closely adjacent electrodes comprising a substrate (Element 323, 223, 403), a first electrode (left of Elements 236, 436) which has a first thickness, a second electrode (right of Elements 236, 436) which has a second thickness, a third electrode (Element 214, 414) which has a third thickness in a hole in the substrate (Figs. 2-4 show the gate electrode in the substrate hole). The third electrode is positioned within the separation between the first and second electrodes (Figs. 2-4). An insulator (Element 202, 402) is on the third electrode. An organic semiconductor (Element 247, 447) is on the first electrode, the second electrode and the insulator.

Zhang does not teach that the separation between the first and second electrodes is about ten nanometers. However, Mizusaki teaches an organic transistor with the channel length being on the nanometer scale such as 1-20 nm (Page 51, Lines 5-8 and 12-13), and

as such the distance between the first and second electrodes being 1-20 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the channel length and hence distance between the first and second electrodes to be about 10 nm. One would have been motivated to do so since Mizusaki teaches that a transistor having such dimensions in the nanometer range, including 10 nm, provides greatly improved characteristics compared to conventional transistors. It has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum value involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). See MPEP § 2144.05.

Zhang does not teach that a sealing layer is on the organic semiconductor and that the first and second thicknesses are at least approximately twice the third thickness. However, Hirai teaches a bottom gate transistor with a sealing layer (Element 4 in Figs. 1-2 and 6) on the organic semiconductor (Element 3 in Figs. 1-2 and 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a sealing layer on the organic semiconductor as taught by Hirai in the device of Zhang. One would have been motivated to do so since Hirai teaches that the sealing layer protects and stabilizes the organic semiconductor and its contact to the source and drain electrodes (see Col. 7, Lines 24-30) and deterioration of the organic semiconductor due to light can be suppress (see Col. 8, Lines 45-47). Hirai further teaches that the first electrode gate is 200 nm thick (see Col. 18, Line 25) and the sealing layer is 5 microns (see Col. 18, Lines 44-45). While Hirai is not explicit that the first and second electrode source/drains are at least twice the gate thickness, Hirai does teach that they protrude all

of the way through the sealing layer thickness of 5 microns. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first and second electrode source/drains to be at least 5 microns thick, so they protrude from the sealing layer as shown (see Hirai Figs. 1-2 and 6), thereby enabling electrical connection to the outside. It has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Since the first and second electrode source/drains to be at least 5 microns thick and the gate electrode is 200 nm thick, then the claim limitation of the first and second thicknesses being at least approximately twice the third thickness is met.

b. Regarding claim 20, Zhang teaches that the substrate comprises polymer (see Para. 0009, Lines 46 and 49 and Para. 0011, Line 3)

c. Regarding claim 21, Zhang teaches that the first electrode comprises gold (see Para. 0009, Line 41 and Para. 0012, Line 10).

d. Regarding claim 22, Zhang teaches that the third electrode comprises gold (see Para. 0009, Line 41, for example).

e. Regarding claim 27, the language of the claim is directed towards the process of making the electronic component of claim 19. It is well settled that "product by process"

limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. As such, the language claim 27 only requires the structure of the electronic device of claim 19, which does not distinguish the invention from Zhang in view of Mizusaki in view of Hirai, who teaches the structure as claimed. The claim does not add any additional structural features to the final device that are not already set forth by claim 19.

5. Claims 23-25 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (`935) in view of Mizusaki (WO `640; supplied with Office Action dated 11 September 2009) in view of Hirai (`900) in view of in view of Higuchi (J. Poly. Sci., Part B: Poly. Phys., Vol. 34; provided as evidence and supplied with Office Action dated 28 April 2009).

f. Regarding claim 19, Zhang teaches an electronic component as a bottom gate transistor with closely adjacent electrodes comprising a substrate (Element 323, 223, 403), a first electrode (left of Elements 236, 436) which has a first thickness, a second electrode (right of Elements 236, 436) which has a second thickness, a third electrode (Element 214, 414) which has a third thickness in a hole in the substrate (Figs. 2-4 show the gate electrode in the substrate hole). The third electrode is positioned within the separation between the first and second electrodes (Figs. 2-4). An insulator (Element 202, 402) is on the third electrode. An organic semiconductor (Element 247, 447) is on the first electrode, the second electrode and the insulator.

Zhang does not teach that the separation between the first and second electrodes is about ten nanometers. However, Mizusaki teaches an organic transistor with the channel length being on the nanometer scale such as 1-20 nm (Page 51, Lines 5-8 and 12-13), and as such the distance between the first and second electrodes being 1-20 nm. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the channel length and hence distance between the first and second electrodes to be about 10 nm. One would have been motivated to do so since Mizusaki teaches that a transistor having such dimensions in the nanometer range, including 10 nm, provides greatly improved characteristics compared to conventional transistors. It has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum value involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). See MPEP § 2144.05.

Zhang does not teach that a sealing layer is on the organic semiconductor and that the first and second thicknesses are at least approximately twice the third thickness. However, Hirai teaches a bottom gate transistor with a sealing layer (Element 4 in Figs. 1-2 and 6) on the organic semiconductor (Element 3 in Figs. 1-2 and 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a sealing layer on the organic semiconductor as taught by Hirai in the device of Zhang. One would have been motivated to do so since Hirai teaches that the sealing layer protects and stabilizes the organic semiconductor and its contact to the source and drain electrodes (see Col. 7, Lines 24-30) and deterioration of the organic semiconductor due to light can be suppress (see Col. 8, Lines 45-47). Hirai further teaches that the first electrode gate is 200 nm thick (see Col. 18, Line 25) and the sealing layer is 5 microns (see Col. 18, Lines 44-45). While Hirai is not explicit that the first and second electrode source/drains are at least twice the gate thickness, Hirai does teach that they protrude all of the way through the sealing layer thickness of 5 microns. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first and second electrode source/drains to be at least 5 microns thick, so they protrude from the sealing layer as shown (see Hirai Figs. 1-2 and 6), thereby enabling electrical connection to the outside. It has been held that where the general conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Since the first and second electrode source/drains to be at least 5 microns thick

and the gate electrode is 200 nm thick, then the claim limitation of the first and second thicknesses being at least approximately twice the third thickness is met.

Zhang teaches the specific materials used as a flexible film for the insulating layer (Elements 202, 402) which includes, for example, polycarbonate (see Para. 0009, Line 33), but does not teach that these materials are used for flexible film as the substrate (Elements 223, 323, 423). However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same materials for the substrate as the insulating flexible film, such as polycarbonate, thereby streamlining the manufacturing process by economy of scale and because these are functionally equivalent materials for a flexible film suitable in organic transistor fabrication. It has been held that the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945). See also *In re Leshin*, 227 F.2d 197, 125 USPQ 416 (CCPA 1960). MPEP § 2144.07. Higuchi evidences that polycarbonate is a glass (see Higuishi who states that polycarbonate is a polymer glass), which is a glass that is different than SiO_2 (see Higuchi "PC glasses").

g. Regarding claim 24, Zhang teaches that the substrate comprises polymer (see Para. 0009, Lines 46 and 49 and Para. 0011, Line 3)

h. Regarding claim 25, Zhang teaches that the first electrode comprises gold (see Para. 0009, Line 41 and Para. 0012, Line 10).

i. Regarding claim 28, the language of the claim is directed towards the process of making the electronic component of claim 23. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. As such, the language claim 27 only requires the structure of the electronic device of claim 19, which does not distinguish the invention from Zhang in view of Mizusaki in view of Hirai in view of Higuishi, who teaches the structure as claimed. The claim does not add any additional structural features to the final device that are not already set forth by claim 23.

Allowable Subject Matter

6. Claims 2, 13 and 26 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: A search of the prior art does not disclose or reasonably suggest a method for producing, on a substrate, an electronic component with closely adjacent electrodes, the method comprising: depositing a first metal layer onto the substrate; structuring a first photo lacquer on a surface of the first metal layer, wherein a portion of the surface of the first metal layer does not have the first photo lacquer thereon; etching the portion of the surface of the first metal layer not having the first photo lacquer; undercut etching the first metal layer so that an overhang is defined by the first photo lacquer; exposing, to a metal vapor, a surface of the first photo lacquer and an exposed portion of the substrate where the first metal layer was etched away so that a second metal layer is formed on the surface of the first photo lacquer and the exposed portion of the substrate where the first metal layer was etched away except in a space between the overhang and the substrate; and removing both the first photo lacquer and the second metal layer formed on the surface of the first photo lacquer; etching a hole into the substrate at a position other than a position of the first metal layer and the second metal layer; depositing a third metal layer onto the substrate, the first metal layer, and the second metal layer; applying an insulator onto the third metal layer; applying an organic semiconductor onto the third metal layer and the insulator; and applying a sealing layer onto the organic semiconductor.

Response to Arguments

8. Applicant's arguments with respect to claims 19-25 and 27-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Hirose (JP `952) teaches a method of forming a thin film transistor with a gate electrode in a hole in a substrate.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW W. SUCH whose telephone number is (571)272-8895. The examiner can normally be reached on Monday - Friday 9AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kiesha Bryant can be reached on (571) 272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew W. Such/
Examiner, Art Unit 2891